**UNIT II**

**Flip Flops, Multivibrators and their applications**

**Flip Flop:**

Any device or circuit that has two stable states is said to be bistable. A flip flop is a bistable electronic circuit that has two stable states. The two stable states are 0 and +5V dc. Flip flop also has memory since its output will remain as SET until something is done to change it. So flip flop is regarded as memory a device. In fact any bistable device can be used to store one binary bit. For instance, when the Flip Flop has its output set at 0V dc, it can be regarded as storing logic 0 and when its output is SET at + 5V dc, it is regarded as storing logic 1.

**R-S Flip Flop:**

Figure shows conventional diagram of R S Flip Flop. It is constructed using two NOR gates. The truth table for NOR gate is shown in Table 1.



**FIG1: R-S Flip Flop using NOR Gate**

The Flip Flop has two outputs Q and Q’. There are two inputs defined as R and S. The input/output possibilities for R S Flip Flop are summarized in Table 2.

|  |  |
| --- | --- |
| Introduction to NOR Gate - projectiot123 Technology Information Website  worldwide | Difference between SR Flipflop and RS Flipflop ? | InstrumentationTools |

 **Table 1: Truth table for NOR Gate** **Table 2: Truth table for R-S Flip Flop**

The first input condition in the truth table is R=S=0. Since 0 input at NOR gate has no effect on the output and Flip Flop will remain in its last state and the output remains unchanged.

The second input condition R = 0 and S = 1, forces the output of NOR gate B to go low. Thus both the inputs to NOR gate A are low. Hence its output is high. Thus 1 at S input is said to SET flip flop and the flip flops switches to the stable state where Q=1.

The third input condition is R = 1 and S = 0. This input forces the output of NOR gate A to go low, since both the inputs to NOR gate B are now low, the output is forced to go high. Thus 1 at R input is said to RESET the flip flop and flip flops switches to stable state Q=0.

The last input condition in the table is equal R=S=1. This is a forbidden condition as it forces the output of both the NOR gates to go low. In other words both Q and Qbar are forced to to be zero at the same time. But this violates the basic definition of flip flop so this input condition is a forbidden condition and it is never imposed.

**Clocked RS flip flop**

THE RS flip flop is called LATCH or Bistable multivibrator. Fig. shows circuit diagram of clocked R S flip flop.



 **FIG 2: CLOCKED R-S Flip Flop**

The addition of two AND gates at R and S inputs will result in a flip flop that cab be ENABLED or DISABLED whenever required. When ENABLED input is low, the output of both the AND gates will be low and changes in neither R nor S will have any effect on the output of flip-flop that is Q. And the flip-flop or latch is said to be disabled.

When ENABLE input is high, information at R and S input will be directly transmitted to the output. The output will change in response to the input condition as long as ENABLE input is high. When S is high, Q will be high and when S is low, Q will be low.

When ENABLE input goes low, the output will retain the information that was present on the input when high to low transmission takes place.

**D Flip Flop**

The R S Flipflop has two data inputs. Generation of two signals to drive a flip flop is a disadvantage in many applications. Further, more the forbidden condition of both the R and S high may occur inadvertently. This led to D Flip flop, a circuit that needs only a single data input. Figure shows a simple way to build delay (D) Flipflop. This kind of flipflop prevents the value of D from reaching the Q output until the clock pulse occurs.

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D-type Flip Flop Counter or Delay Flip-flop |

|  |
| --- |
| **Truth Table of D** **Flip Flop** |
| Clk | D | Q |
| ↓ | x | Last state |
| ↑ | 1 | 1 |
| ↑ | 0 | 0 |

 |

**FIG 3: A simple way to build delay (D) Flip flop.**

This kind of flip flop prevents the value of D from reaching the Q output until the clock pulse occurs. When the clock is low, both the AND gates are disabled therefore D can change value without affecting the value of Q. On the other hand, when clock is high, both the AND gates are enabled and, in this situation, Q is forced to equal to the value of D input i.e. when D is high, Q is high and when D is low, Q is also low. When clock goes low, Q retains or stores the last value of Q.

**Edge triggered D- Flip flop:**

Although D latch is used for temporary storage in electronic instruments, an even more popular kind of D Flip flop is used in digital computers and systems. This kind of flip flop samples the data bit at a unique point of time.



**FIG 4: R C circuit to convert Square wave to spikes**

By deliberate design the RC time constant (Ʈ=0.69 RC) is kept much smaller than clock pulse width. Because of this the capacitor can charge fully when clock goes high. This exponential charging produces a narrow positive voltage spike across the resistor. Later trailing edge of the pulse results in a narrow negative spike. This is called RC differentiation.

 D Input

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 **Edge triggered D Flip Flop**

Figure shows a RC circuit at the input of D latch. The narrow positive spike enables the AND gate for an instant, while the narrow negative spike does nothing. The effect is to activate the AND gate during the positive spike equivalent sampling the values of D for an instant. At this unique point of time, D and its complement hit the flip flop inputs forcing Q to SET or RESET depending on the values of D input.

This kind of operation is called edge triggering because the flip flop responds only when the clock is in transition between two voltage states. The triggering occurs on the positive going edge of the clock, this is why it is referred to as positive edge triggering.

The truth table summarizes the action of positive edge triggered D flip flop.

|  |
| --- |
| **Truth Table of Edge Triggered D Flip Flop** |
| Clk | D | Q |
| ↓ | x | Last state |
| ↑ | 1 | 1 |
| ↑ | 0 | 0 |

On the leading edge of the clock, designated by the up arrow (↑) the data bit is loaded into the flip flop and Q takes the value of D. On the trailing edge of the clock, D is don’t care (x) and Q remains in its last state.

When power is first applied, the flip flops come in random state. To get some computers started an operator has to push RESET button. This sends a CLEAR or PRESET signals to all flip flops.



**FIG 5: Edge triggered D Flip Flop with PRESET and CLEAR facilities**

Figure shows how to include both functions in a D flip flop. The OR gate allows us to slip in a high PRESET and a high CLEAR when desired. A high PRESET forces Q to be equal to 1 and high CLEAR forces Q to be zero. PRESET and CLEAR are Asynchronous inputs because they activate the flip flops independently of the clock pulse. On the other hand, D input is a synchronous input because it has an effect only when clock edge occurs.

**J K Flip Flop:**

Flip flops are used to build counters, a circuit that counts the number of positive or negative clock edges driving its clock input. For purpose of counting, the J K flip flop is an ideal element to use.




**FIG 5: J K Flip Flop symbol, Circuit and Truth Table**

Figure 6 shows one way to build J K flip flop. The variables J and K are called control inputs because they determine what flip flop does when a positive clock edge arrives. The RC circuit has time constant (Ʈ) less than the clock width (T), thus converting rectangular clock pulse into a narrow spike. Because of AND gate the circuit is called positive edge triggered.

When J and K are both low, AND gates are disabled. Therefore, clock pulses have no effect. This first possibility is the initial entry in the truth table. When J and K are both low, Q retains its last state.

When J is low and K is high, the upper AND is disabled. So, there is no way to SET the flip flop. The only possibility is to RESET. When Q is high, lower gate passes a RESET trigger as soon as next positive clock edge arrives. This forces Q to become low.

When J is high and K is low, the lower gate is disabled. So, it is impossible to RESET the flip flop. But we can SET the flip flop. When Q is low, $\overbar{Q }$is high. Therefore, upper gate passes a SET trigger on the next positive clock edge. This drives Q into high state and thus when J=1 and K=0 means that on next positive clock edge the flip flop SETS.

When J and K are both high, it’s possible to SET or RESET the flipflops. If Q is high, then lower gate passes a RESET trigger on the next positive clock edge. On the other hand, if Q is low then $\overbar{Q }$ passes a SET trigger on the next positive clock edge. In either way, Q changes to the complement of the previous state. Therefore, J=K=1 means the flip flop will toggle on the next positive clock edge. Toggle means to switch to opposite state.

Propagation delay prevents the J K flip flop from racing (Toggling more than once during the positive clock edge). The output changes after the positive clock edge have struck. By then Q and $\overbar{Q }$ values are too late to coincide with the positive spikes driving the AND gate.

If tp =20 ns, the output change approximately 20 ns after the leading edge of the clock pulse. If the clock strikes are narrower than 20 ns, then returning Q and $\overbar{Q }$ arrives too late to cause false triggering.

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| --- | --- | --- |
|  |  | JK-Flip Flop Evolution |
| Positive edge triggered JK Flip flop | Positive edge triggered JK Flip flop with positive PRESET and CLEAR facility | Negative edge triggered JK Flip flop with negative PRESET and CLEAR facility |

**FIG 6: Various symbols of J K Flip Flop**

**J K Master Slave Flip Flop:**

Figure 7 shows one way to build J K Master Slave Flip flop. It provides another key or method to avoid racing problem.

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| --- | --- |
| Todays Circuits ~ Engineering Projects | : Master-Slave Flip Flop Circuit |  |

**FIG 7: J K Master Slave Flip flop with Truth Table**

To begin with, the master is positive edge triggered and the slave is negative edge triggered. Therefore, Master responds to its J and K inputs before the slave. If J=1 and K=0, the master SETS on the leading edge of the clock pulse. The high Q output of the master drives J input of the slave and $\overbar{Q }$ drives K input of the slave. So, when the trailing edge of clock pulse hits slave, the slave SETS copying the master.

If J=0 and K=1, the master RESETS on the leading edge of the clock. The high $\overbar{Q }$ output of the master goes to the K input of the slave. Therefore, the on arrival of trailing edge of the clock pulse, it forces the slave to RESET. Again, the slave has copied the master.

If master’s J and K both inputs are high, it toggles on the positive clock edge and the slave toggles on the negative clock edge. Thus, regardless of what master does, the slave always copies the master.

**Multivibrators:**

Multivibrator is a regenerative circuit consisting of two active devices, wired or inter connected in such a way that when one active device is in saturation then other is in cut off and vice versa. There are three types of multivibrators. (i) Astable multivibrator (ii) Monostable multivibrator (iii) Bistable multivibrator.

**Astable Multivibrator:** A multivibrator circuit having **no** stable state is called Astable multivibrator.

**Monostable Multivibrator:** A multivibrator circuit having **one** stable state is called Monostable multivibrator.

**Bistable Multivibrator:** A multivibrator circuit having **two** stable state is called Bistable multivibrator.

**Schmitt Trigger:**

The Schmitt trigger multivibrator has got two stable states and hence it is Bistable multivibrator. However, instead of coupling from the collector of one transistor to the base of another, it couples by the way of common emitter resistor.



**FIG 8: Circuit Diagram of Schmitt Trigger**

The coupling is done in such a way that when Q1 conducts Q2 is OFF and when Q2 conducts Q1 is OFF.

To understand how circuit works, assume the input voltage Vin id set to 0V. Under this condition, no base current flows in Q1. Therefore, there is no collector current in Q1. But collector voltage of Q1 is maximum (Vcc). The base of Q2 is connected to a voltage divider formed by 100 KΩ resistor. The volage at the top of the divider is enough to turn the base ON and saturate Q2. With Q2 saturated its collector and emitter are effectively shorted. As a result the voltage from collector to emitter will be 2V.

With the input battery at 0V, we have Q1 cut off and Q2 saturated. Under this condition, output voltage of Schmitt trigger is 2V. Since emitter voltage is 2V, no base current can flow in Q1 for Vin less than 2V. Thus output of Schmitt Trigger remains 2V till Q2 is saturated.

If we raise the input voltage above 2V, base current flows in Q1. Once this happens, collector current begins to flow and voltage at Q1 collector decreases. This makes Q2 to come out of saturation and its collector voltage increases. This makes Q1 to conduct more heavily and it reaches saturation. With Q1 saturated its collector voltage is 0V and this cuts off Q2. So, the output voltage of Q2 becomes 10 V. Thus the output of Schmitt trigger swings from 2V to 10 V.

With Q1 saturated, the emitter to ground voltage is 1V. So, only one way to bring Q1 out of saturation is to reduce Vin voltage below 1 V. This will drive Q1 back to cut off and Q2 to saturation.

The output of Schmitt trigger circuit is as shown in figure 9.



**FIG 9: Output of Schmitt Trigger circuit**

The value of Vin that causes the output to jump from low state to high state is called **Upper trip point (UTP)**. The value of Vin that causes the output to jump from high state to low state is called **lower trip point (LTP)**. The difference between UTP and LTP is called **hysteresis**. Hysteresis is very beneficial feature because it can be used to provide noise immunity.

Schmitt trigger has many important applications.

1. It is used as voltage comparator circuit.
2. It is used as wave shaping circuit.
3. It is used as signal conditioning device.

**Astable Multivibrator:**

Astable multivibrator has no stable state and hence it is also called free running multivibrator. It is widely used for generation of pulses, either square wave or rectangular wave depending on the choice of circuit components.



 FIG 10: Astable Multivibrator

A typical free running multivibrator is shown in the figure. The circuit consists of two stage RC coupled amplifier with output of second stage coupled back to the input of first stage via capacitor C2 and output of TR1 coupled to TR2 via capacitor C1. The circuit is symmetrical with equal values of load resistors, capacitors and base resistors.

When power is first applied the transistor whose β value (current gain) is high will go to saturation first and other will go to cut off. Suppose Q1 has β value slightly higher than TR2. So TR1 will go to saturation and TR2 will go to cut off. With Q1 saturated its collector voltage is practically 0V and with TR2 cut off its collector voltage is Vcc.

With TR1 saturated, capacitor TR2 is at 0V so it will start charging to VBB via resistor R2 and so successively TR2 will go to saturation and TR1 will go to cut off. This is cumulative process. The waveforms obtained at each collector will be square wave and its frequency is $f=\frac{0.7}{RC}$, where R is value of base resistor and C is value of coupling capacitor.

**Monostable Multivibrator:**

This kind of multivibrator is stable in one state but unstable in the other. It is called One Shot multivibrator. When triggered it goes from stable state to unstable state temporarily and then returns to stable.

Figure 11 shows general idea of Monostable multivibrator. At a point A in time a trigger hits the input. This causes the output voltage to go from low state to high state. This high state is unstable so after a while the output voltage returns to the low state



 Figure: Monostable Multivibrator

**FIG 11: Monostable Multivibrator**

The low state has Q1 OFF and Q2 saturated. When positive trigger arrives, it turns Q1 ON which drops collector voltage of Q1. This drop couples to the base of Q2 shutting this transistor OFF. But this condition Q1 ON and Q2 OFF is temporary. After an amount of time determined by the RC time constant of base current, Q2 again turns ON and Q1 turns OFF.

Each time a positive trigger hits the base of Q1, the output voltage Y goes from low to high temporarily but then returns to a low state.